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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/870,800	06/01/2001	Richard S. Norman	13689	8344

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EXAMINER	
LEE, ANDREW CHUNG CHEUNG	
ART UNIT	PAPER NUMBER
2616	

DATE MAILED: 06/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/870,800	NORMAN ET AL.	
	Examiner	Art Unit	
	Andrew C. Lee	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16,18-21 and 31-43* is/are rejected.

7)☒ Claim(s) *17,22,23,24,25,26,27,28,29,30,44* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 – 8, 11 – 16, 18 – 21, 31 – 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Chang et al. (US 6731631 B1) in view of Oguchi (US 6907042 B2).

Regarding **Claim 1**, Chang et al. disclose the limitation of a switch fabric implemented on a chip (recited "switch fabric chipset system" as a switch fabric implemented on a chip; Fig. 1, column 5, line 33), comprising: a) an array of cells (recited "a plurality of switch fabric components" as an array of cells; column 6, element 104, line 2; lines 7 – 11); b) an I/O interface in communication with said array of cells for permitting exchange of data packets between said array of cells and components external to said array of cells (recited "a plurality of port controllers interconnected to one another" as an I/O interface in communication with said array of cells; column 5, lines 64 – 67, column 6, lines 1 – 14); c) each cell communicating with at least one other cell of said array permitting exchange of data packets between the cells of said array (recited "a plurality of switch fabric components (recited as cells) connected together via bi-directional conduits" as each cell communicating with at least one other cell of said array; column 6, lines 1 – 9); d) each cell including: I) a memory for receiving a data packet from

another cell of said array (recited " packet memory" as a memory for receiving a data packet; Fig.2, Fig.3, elements "Packet Memory and Lookup Memory"); Chang et al. also teach the free cell manager manages the free cells in the memory of the switch matrix based on the information provided via the central controller and maintains the information about the occupied cells and the free cells in the switch matrix in a table (column 16, lines 34 – 40). Chang et al. do not disclose explicitly a control entity to control release of a data packet toward a selected destination cell of said array at least in part on a basis of a degree of occupancy of the memory in said destination cell. Oguchi discloses the limitation of a control entity (recited "reassembly buffer processor" as a control entity) to control release of a data packet toward a selected destination cell of said array at least in part on a basis of a degree of occupancy of the memory in said destination cell (recited "the free space notifying portion allocated in the upper layer can detect the free space of the receiving buffer" as control release of a data packet toward a selected destination cell of said array at least in part on a basis of a degree of occupancy of the memory in said destination cell; column 6, lines 39 – 48, lines 53 – 60). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Chang et al. to include a control entity to control release of a data packet toward a selected destination cell of said array at least in part on a basis of a degree of occupancy of the memory in said destination cell such as that taught by Oguchi in order to provide a backward packet inclusive information reading circuit for detecting the free space based on information within backward packet from the upper layer (as suggested by Oguchi, see column 6, lines 44 – 47).

Regarding claim 2, Chang et al. disclose the limitation of a switch fabric (recited "switch fabric chipset system" as a switch fabric; Fig. 1, column 5, line 33; column 15, line 35) as defined in claimed wherein each cell of said array (recited "switch fabric component" as each cell; Fig. 20, element 2000, column 15, lines 38 – 44) includes: a) a transmitter in communication with said I/O interface (recited "interface transmitter" as a transmitter in communication with said I/O interface; Fig. 20, element 2006, column 16, lines 9 –13) and in communication with every other cell of said array (recited "connectable to the interface receiver of another switch fabric component" as communication with every other cell of said array; column 16, lines 9 –13), said transmitter operative to process a data packet received from said I/O interface to determine a destination of the data packet and forward the data packet to at least one cell of said array selected on a basis of the determined destination (recited "each interface transmitter interacts with central controller for control, the central controller reads the destination port from the destination vector of a packet" as said transmitter operative to process a data packet received from said I/O interface to determine a destination of the data packet; column 16, lines13 – 19; lines 29 – 32); b) a plurality of receivers associated with respective cells from said array (recited "the switch fabric component includes an interface receiver" as receiver with respective cell; Fig. 20, element 2002, column 15, lines 38 – 44, 47 – 50), each receiver being in communication with a respective cell allowing the respective cell to forward data packets to the receiver (recited "interface receiver serves to receive packets, ..to permit transferring of a received packet from the interface receiver to the switch matrix" as each receiver being in communication with a respective cell allowing the respective cell to forward data packets to the receiver; column 15, lines 58 – 61); c) said receivers in communication with said I/O interface

for releasing data packets to said I/O interface (recited "each incoming packets is stored in memory of the switch matrix until the packet can be transferred to an interface transmitter for transmission out of the switch fabric component" as receivers in communication with said I/O interface for releasing data packets to said I/O interface; column 15, lines 66 – 67; column 16, lines 1 – 6).

Regarding claims 3 and 4, Chang et al. disclose the limitation of a switch fabric as defined in claimed, wherein said array of cells includes a plurality of data channels (recited " switch matrix provides a data path for packets in the switch fabric component" as array of cells includes a plurality of data channels; column 15, lines 50 – 67), each data channel being associated with a given cell (recited "a switch fabric component may include more than one interface receiver and more than one interface transmitter" as each data channel being associated with a given cell; column 15, lines 43 – 49), the data channel associated with said given cell connecting the transmitter of said given cell to receivers in cells other than said given cell and associated with said given cell (column 15, lines 58 – 61; lines 66 – 67; column 16, lines 1 – 2).

Regarding claim 5, Chang et al. disclose the limitation of a switch fabric as defined in claim 4, wherein the plurality of data channels are independent from one another (recited "one conduit for each port controller" as data channels are independent from one another; column 6, lines 44 – 47), wherein transmission of a data packet over one data channel is made independently of a transmission of a data packet over another data channel (recited "path from every port controller to all of the other port controllers not directly coupled to the same switch

fabric components" as transmission of a data packet over one data channel is made independently of a transmission of a data packet over another data channel; column 6, lines 55 – 59; column 8, lines 15 – 18; Fig. 10, column 11, lines 45 – 48).

Regarding claim 6, Chang et al. disclose the limitation of a) A switch fabric as defined in claim 5, wherein each data channel performs a parallel data transfer (recited "processing and storing of a plurality of incoming packets" as each data channel performs a parallel data transfer; Fig. 10, elements 1002, 1004, 1006 and 1008; column 11, lines 45 – 48).

Regarding claim 7, Chang et al. disclose the limitation of a switch fabric as defined in claim 1, wherein said array of cells forms a matrix (recited "switch matrix" as array of cells forms a matrix; Fig.1, column 15, line 67; column 16, lines 1 – 2; lines 9 – 13).

Regarding claim 8, Chang et al. disclose the limitation of a switch fabric as defined in claim 7, wherein said matrix is bi-dimensional (recited "connections are bi-directional" as di-dimensional; column 6, lines 2 – 4).

Regarding claim 11, Chang et al. disclose the limitation of a switch fabric as defined in claim 2, wherein said memory is a first memory (Fig. 3, packet memory of element 302a) and wherein the transmitter of said given cell includes a second memory for storing data packets received from said I/O interface (Fig. 3, packet memory (16M) of element 302b).

Regarding Claim 12, Chang et al. disclose the limitation of a switch fabric as defined in claim 11, wherein said second memory includes a plurality of segments (Fig. 17, elements 1702, 1704, 1706 and 1708; column 14, lines 34 – 37), each segment being associated with a receiver in a cell of said array to which the transmitter of said given cell is capable of forwarding a data packet via the data channel (column 14, lines 37 – 39; column 14, lines 58 – 61; column 15, lines 6 – 10).

Regarding claim 13, Chang et al. disclose the limitation of a switch fabric as defined in claim 12, wherein the transmitter of said given cell includes said control entity (recited "port controller" as the transmitter of said given cell includes said control entity; column 16, lines 14 – 19), said control entity being operative to process a data packet forwarded from said I/O interface to determine a cell of said array to which the data packet is destined (recited "central controller manages the storing of incoming packets" as control entity being operative to process a data packet; column 16, lines 21 – 29) and identify on a basis of the determined cell a segment of said second memory into which the packet is to be loaded(recited "reads the destination port from the destination vector of a packet and stores the packet in a queue" as identify on a basis of the determined cell a segment of said second memory into which the packet is to be loaded; column 16, lines 24 – 32).

Regarding claim 14, Chang et al. disclose the limitation of a switch fabric as defined in claim 13, wherein said control entity includes a plurality of queue controllers associated with

respective segments of said second memory (recited "queue manager" as queue controller; column 16, lines 42 – 47).

Regarding claim 15, Chang et al. disclose the limitation of a switch fabric as defined in claim 14, wherein said second memory implements a plurality of registers (Fig. 17, elements 1710, 1714, 1718), each register being associated with a queue controller (column 16, lines 42 – 47) and being suitable for holding data representative of a degree of occupancy of a segment of said second memory associated with the queue controller (column 16, lines 33 – 40).

Regarding claim 16, Chang et al. disclose the limitation of a switch fabric as defined in claim 15, wherein a data packet received by said transmitter from said I/O interface is characterized by a priority level selected in a group of priority levels (recited "assigned output priority queues" as transmitter from said I/O interface is characterized by a priority level selected in a group of priority levels; column 14, lines 32 – 37), each segment of said second memory being partitioned into slots (recited "output orientated scheduler has a plurality of output priority queues" as each segment of said second memory being partitioned into slots; column 14, lines 34 – 39), each slot capable of storing at least one data packet (column 14, lines 44 – 46), each slot being associated with a given priority level of said group of priority levels (recited "each cell points a the address where next cell is saved" as each slot being associated with a given priority level of said group of priority levels; column 14, lines 47 – 54).

Regarding claim 18, Chang et al. disclose the limitation of a switch fabric as defined in claim 13, wherein said first memory is divided into a plurality of sectors associated with respective ones of said receivers (Fig. 14, column 13, lines 1 – 10), said sectors capable of storing data packets forwarded to said receivers by cells of said array (column 13, lines 11 – 18), said control entity being operative to communicate with each receiver associated with said given cell to assess a degree of occupancy of the sector of each receiver associated with said given cell (column 16, lines 42 – 47).

Regarding claim 19, Chang et al. disclose the limitation of a switch fabric as defined in claim 18, wherein said control entity communicates with each receiver associated with said given cell to assess the degree of occupancy of the sector of each receiver associated with said given cell, over a back channel (Fig. 33. element 3300, column 5, lines 52 – 55; column 23, lines 51 – 55).

Regarding claim 20, Chang et al. disclose the limitation of a switch fabric as defined in claim 19, including a plurality of back channels (Fig. 33, elements 3306, 3304, 3302), there being a dedicated back channel between said control entity and each receiver associated with said given cell (Fig. 33, column 24, lines 29 – 36).

Regarding claim 21, Chang et al. disclose the limitation of a switch fabric as defined in claim 20, wherein each back channel transfers data serially (recited "back propagation" as back channel; column 23, lines 56 – 57).

Regarding claim 31, Chang et al. disclose the limitation of a switch fabric as defined in claim 18, wherein each receiver of said plurality of receivers communicates with said I/O interface (column 15, lines 55 – 56).

Regarding claim 32, Chang et al. disclose the limitation of a switch fabric as defined in claim 31, wherein said control entity is a first control entity (Fig. 20, element 2008a, column 15, lines 63 – 65) and wherein said plurality of receivers include a second control entity to regulate a release of data packets from said sectors to said I/O interface (column 16, lines 24 – 32).

Regarding claim 33, Chang et al. discloses the limitation of a switch fabric as defined in claim 32, wherein said second control entity includes a plurality of queue controllers associated with respective sectors of said first memory (Fig. 20, element 2012, column 16, lines 42 – 47).

Regarding claim 34, Chang et al. disclose the limitation of a switch fabric as defined in claim 33, wherein a data packet received by a receiver of said plurality of receivers is characterized by a priority level selected in a group of priority levels (column 13, lines 44 – 45), each sector of said second memory being divided into subdivisions (column 13, lines 57 – 58), each subdivision capable of storing at least one data packet (column 14, lines 1 – 2), each subdivision being associated with a given priority level of said group of priority levels (Fig. 17, column 14, lines 34 – 37).

Regarding claim 35, Chang et al. disclose the limitation of a switch fabric as defined in

claim 34, wherein said second control entity includes an arbiter in communication with said queue controllers (Fig. 20, element 2012, column 16, lines 42 – 47), each queue controller operative to transmit a control signal to said arbiter for each data packet held in the sector associated with the queue control to request release of the data packet to said I/O interface (column 14, lines 10 – 23).

Regarding claim 36, Chang et al. disclose the limitation of a switch fabric as defined in claim 35, wherein each control signal conveys the priority level of the data packet associated with the control signal (column 13, lines 66 – 67; column 14, 2 – 6).

Regarding claim 37, Chang et al. disclose the limitation of a switch fabric as defined in claim 36, wherein said arbiter selects a data packet for release to said I/O interface among the data packets corresponding to the control signals transmitted to said arbiter on the basis of the levels of priority of the data packets corresponding to the control signals transmitted to said arbiter (Fig. 17, column 14, lines 31 – 47).

Regarding claim 38, Chang et al. disclose the limitation of a switch fabric as defined in claim 2, wherein each data packet comprises a plurality of words including a first word of said data packet and a last word of said data packet (Fig. 6, element 600; lines 55 – 58), wherein each word comprises a field indicative of whether said word is a pre-determined number of words away from said last word of said data packet (Fig. 6, element 610 (length); column 10, lines 55 – 58).

Regarding claim 39, Chang et al. disclose the limitation of a switch fabric as defined in claim 38, wherein the transmitter is operative to monitor said field in each word of each data packet forwarded to at least one cell of said array (Fig. 8, column 11, lines 11 – 20), the transmitter further being operative to begin forwarding a next data packet upon detecting that said field of a word in a packet currently being forwarded is indicative of said word being a pre-determined number of words away from the last word of said data packet currently being forwarded (Fig. 10, column 11, lines 45 – 54).

Regarding claims 40, 41, Chang et al. disclose the limitation of a switch fabric as defined in claim 3, each cell further including a central processing unit (CPU) connected to the transmitter (Fig. 20, element 2008 (2008a, 2008b, 2008c); element 2006; column 15, lines 39 – 43), said transmitter being further operative to process a data packet received from said CPU to determine a destination of the data packet and forward the data packet to at least one cell of said array selected on the basis of the determined destination (column 16, lines 13 – 19), wherein data packets received by the transmitter in a given cell from the I/O interface and from the CPU in said given cell share the data channel associated with said given cell (column 16, lines 24 – 32).

Regarding claim 42, Chang et al. disclose the limitation of a) A switch fabric as defined in claim 2, each cell further including a central processing unit (CPU) connected to the plurality of receivers (Fig. 20, element 2008 (2008a, 2008b, 2008c); element 2006; column 15, lines 39 – 43; lines 47 – 49), said receivers being further operative to determine whether data packets are to

be released to the I/O interface or to the CPU and release said data packets accordingly (column 15, lines 58 – 65).

Regarding claim 43, Chang et al. disclose the limitation of a switch fabric as claimed in claim 42, wherein each data packet comprises a field indicative of whether the data packet is destined for a CPU (column 15, lines 3 – 5) and wherein said receivers are operative to determine whether data packets are to be released to the I/O interface or to the CPU on the basis of said field (column 15, lines 6 – 12).

3. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. (US 6731631 B1) and Oguchi (US. 6907042 B1) as applied to claims 1 – 8, 11 – 16, 18 – 21, 31 – 43 above, and further view of McCrosky et al. (US 6741 552 B1).

Regarding claim 9, Chang et al. and Oguchi do not disclose expressly a switch fabric as defined in claimed wherein said matrix is three-dimensional. McCrosky et al. disclose the limitation of a switch fabric as defined in claimed wherein said matrix is three-dimensional (recited "3 –dimensional binary hypercube" as a switch fabric as defined in claimed wherein said matrix is three-dimensional ; column 28, lines 27 – 51). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Chang et al. and Oguchi to include a switch fabric as defined in claimed wherein said matrix is three-dimensional such as that taught by McCrosky et al. in order to offer a powerful, simple and in many ways elegant

solution to the problem of providing cost-effective, high-bandwidth, fault-tolerant data switching.

Regarding Claim 10, Chang et al. and Oguchi do not disclose expressly a switch fabric as defined in claimed wherein said array of cells forms a toroidal mesh arrangement. McCrosky et al. disclose the limitation of a switch fabric as defined in claim 1, wherein said array of cells forms a toroidal mesh arrangement (column 3, lines 6 – 9). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Chang et al. to include a switch fabric as defined in claimed wherein said array of cells forms a toroidal mesh arrangement such as that taught by McCrosky et al. in order to offer a powerful, simple and in many ways elegant solution to the problem of providing cost-effective, high-bandwidth, fault-tolerant data switching.

Allowable Subject Matter

4. Claims 17, 22, 23, 24, 25, 26, 27, 28, 29, 30, 44 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

5. Applicant's arguments filed on 2/9/2006 with respect to claims 1 – 44 have been fully considered but they are not persuasive.

Conclusion

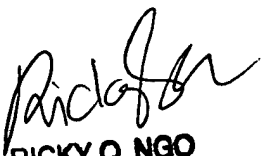
6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew C. Lee whose telephone number is (571) 272-3131. The examiner can normally be reached on Monday through Friday from 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Ngo can be reached on (571) 272-3139. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ACL

June 14, 2006



RICKY Q. NGO
SUPERVISORY PATENT EXAMINER